What is claimed is:

1. A multiprocessor system comprising:

a plurality of processors;

at least one debug executing unit for executing the debugging of said plurality of processors;

at least one controller for controlling said debug executing unit;

a set of terminals to be connected to an external debugging device; and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged.

2. The multiprocessor system according to claim 1, wherein

said plurality of processors comprise first and second processors,

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,

said controller comprises a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit,

said selecting circuit is connected between said first and second controllers and said set of terminals, and

said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided from said debugging device through said set of terminals.

3. The multiprocessor system according to claim 1, wherein

said plurality of processors comprise first and second processors,

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,

said selecting circuit is connected between said first and second debug executing units and said controller,

said controller is connected to said set of terminals, and

said selecting circuit inputs, to one or both of said first and second debug executing units, a debugging signal outputted from said controller.

4. The multiprocessor system according to claim 1, whererin

said plurality of processors comprise first and second processors,

said selecting circuit is connected between said first and second processors and said debug executing unit,

said debug executing unit is connected to said controller,

said controller is connected to said set of terminals, and

said selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit.

5. The multiprocessor system according to claim 1, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of setting of a given register.

6. The multiprocessor system according to claim 1, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis

of a select signal inputted to a given terminal from outside.

7. A multiprocessor system comprising:

first and second processors;

a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor;

a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit;

a first set of terminals selectively connected to said first controller and a second set of terminals selectively connected to said second controller; and

a selecting circuit connected between said first set of terminals and said first and second controllers;

wherein, in a first mode in which debugging devices are connected respectively to said first and second sets of terminals, said selecting circuit connects said first controller and said first set of terminals, and connects said second controller and said second set of terminals,

and wherein in a second mode in which said debugging device is connected only to said first set of terminals, said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal provided from said debugging device through said first set of terminals.

8. The multiprocessor system according to claim 7, wherein said first mode and said second mode are switched on the basis of a select signal inputted to a given terminal from outside.

9. The multiprocessor system according to claim 7, wherein said first mode and said second mode are switched on the basis of setting of a given register.

10. The multiprocessor system according to claim 7, further comprising a detecting circuit for detecting whether said debugging device is connected to said second set of terminals,

wherein said first mode and said second mode are switched on the basis of a result detected by said detecting circuit.